REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed June 11, 2007. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 1-6, 13-25, and 32-38 are pending in the present application. Claims 1-6, 13-25, and 32-38 are rejected under 35 U.S.C. §101 for allegedly being directed to non-statutory subject matter. Claims 1-6, 13-15, 20-25, and 32-34 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Okumura et al.* (U.S. Pat. No. 5,726,923, hereinafter "*Okumura*"). Claims 16-19 and 35-38 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Okumura* in view of Applicants' admitted prior art. Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Response to Claim Rejections Under 35 U.S.C. § 101

Claims 1-6, 13-25, and 32-38 stand rejected under 35 U.S.C. §101 for allegedly being directed to non-statutory subject matter. Specifically, the Office action alleges the following on page 3:

> *Claims 1-6, 13-25, and 32-38 cite a method for determining a minimum/maximum value among values in accordance with a mathematical algorithm. . . [C]laims 1-6, 13-25, and 32-38 merely disclose steps/components for determining minimum/maximum value without further disclosing a practical/physical application or a useful and tangible result.*

As an initial matter, Applicants point out that only claims 13 and 32 recite method claims. (Claims 1, 17, 20, and 36 recite apparatus claims.) Notwithstanding, Applicants submit that the claimed embodiments in these claims do indeed achieve a useful and

tangible result. As discussed in the background section, while priority queues often are useful in scheduling processes, the insertion, removal, and/or maintenance of such priority queues often consumes a considerable portion of the processing cycles of a processor implementing the scheduling process. For example, to determine the minimum value in an unsorted queue, at least one compare instruction and one jump instruction typically are performed for each comparison of a value in the queue to the minimum of the previous values. As such, at least 2n instructions are performed to identify the minimum value and/or its index in the queue. Similarly, for heap data structures, the insertion of a new value (such as when the "due timestamp" for an input queue is modified) into the heap data structure or a removal of a value often necessitates a branch instruction and a jump instruction for each comparison of a parent node to a child node. Since O(log n) comparisons typically are performed when inserting/removing a value into/from a heap data structure of n values, the typical insertion/removal operation takes at least 2 log n cycles to perform. As such, the claimed embodiments are directed to techniques for efficiently determining a minimum of a plurality of values and the index of the minimum using registers of a processor.

The Office Action asserts that claims 1-6, 13-25, and 32-38 "*merely disclose steps/components for determining minimum/maximum value without further disclosing a practical/physical application or a useful and tangible result.*" However, Applicants respectfully point out that one of the cited patent references (*Okumura*) relied upon by the Examiner is directed to a minimum/maximum data detector for rapidly detecting the minimum or the maximum data from a plurality of numeric data. (*See Okumura*,

Abstract.) Accordingly, Applicants respectfully request that the §101 rejection be withdrawn.

II. Response to Claim Rejections Under 35 U.S.C. § 102

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102.

Claims 1-6, 13-15, 20-25, and 32-34 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by *Okumura*. For at least the reasons set forth below, Applicants traverse these rejections.

Independent Claim 1

Applicants respectfully submit that independent claim 1 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the features emphasized below in claim 1.

Claim 1, as amended, recites (emphasis added):

> 1. A processor for determining a minimum value of a plurality of values stored in source registers and determining an index value of a source register having the minimum value, the processor comprising:
> a destination register;
> a first source register storing a first value, ***wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register***;
> a second source register storing a second value, ***wherein the second source register comprises S bits, and wherein the***

second value comprises N lower bits of the second source register;
means for comparing the first value stored in the first source register with the second value stored in the second source register;
means for storing the first value in the destination register when the first value is less than or equal to the second value; and
means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value, ***wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value***.

Applicants have amended claim 1 to further define the claimed embodiment in claim 1 and submit that no new matter is added by the amendment. Applicants submit that the cited *Okumura* reference fails to teach the features emphasized in claim 1 above. Specifically, *Okumura* fails to disclose the following elements: "wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register," "wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register," and "wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value."

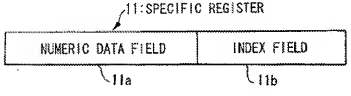
Claim 1 was amended to clarify that for this embodiment, only the N low-order bits of the first and second source registers are compared whereas the remaining high-order bits (*i.e.,* bits [S-1:N]) are not relevant for comparison purposes (where bits [N-1:0] are evaluated). If the second value is less than the first value, the index value is concatenated with the N lower order bits of the second register. The concatenated value is then stored in the destination register.

While *Okumura* discloses registers (5, 6), a counter (9), and a specific register (11), *Okumura* fails to disclose the features emphasized above. At most, *Okumura* teaches the following (emphasis added):

> When a comparing process is executed in the arithmetic logic unit 4, an input numeric data stored in the register 5 and the numeric data field of the specific register 11 arc compared. In this process, the content of the index field of the specific register 11 is disregarded. However, if the index field is located in the lower figures of the numeric data field, and figure matching between two numeric data is made at the input stage of the arithmetic logic unit 4, then the index field would not affect the comparison results. In other words, the content of the specific register 11 can be supplied to the arithmetic logic unit 4 with its original shape and without separating the numeric data field.

(Col. 4, lines 29-40). *Okumura* teaches that the "index field is located in the lower figures of the numeric data field." (*See* FIG. 2 below.)

FIG. 2



However, this is not equivalent to the feature, "wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value." Furthermore, *Okumura* fails to teach the following: "wherein the first value comprises N lower bits of the first source register" and "wherein the second value comprises N lower bits of the second source register."

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the highlighted features in claim 1 above.

Dependent Claims 2-6

Applicants submit that dependent claims 2-6 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 13

Applicants respectfully submit that independent claim 13 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the features emphasized below in claim 13.

Claim 13 recites (emphasis added):

> 13. A method for determining a minimum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:
> for each of the plurality of source registers,
> comparing a value stored in the source register with a value stored in a destination register;
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is less than the value stored in the destination register; and
> ***wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers***.

In alleging that *Okumura* teaches the feature emphasized above, the Office Action asserts the following: "*Figure 2 as general data structure of each specific registers 11x in Figure 4*." (Office Action, page 5). However, Applicants respectfully submit that *Okumura* fails to teach the element, "wherein the destination register *initially* includes an index value and a value *of a first source register* of the plurality of source registers" as *Okumura* specifically teaches that "In FIG. 3, when the operation is started,

an initial value is stored in the specific register 11 in step S1. The initial value is the maximum value (0x7FFF) is identical to step S31 described in the background art (FIG. 6)." (Col. 4, lines 53-56). Referring back to the background section, *Okumura* discloses the following:

> First, a prespecified initial value is stored in the accumulator 7 (S31). When detecting minimum data, the initial value is preferably the maximum value within the expressible scope of the numeric data. For example, if the numeric data are expressed by "16" bits width two's complement data, the initial value is preferably "0x7FFF."

(Col. 1, lines 56-61). *Okumura* teaches that "the initial value is preferably the maximum value within the expressible scope of the numeric data."

Accordingly, Applicants respectfully submit that independent claim 13 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the highlighted features in claim 13 above.

Dependent Claims 14-16

Applicants submit that dependent claims 14-16 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 20

Applicants respectfully submit that independent claim 20 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the features emphasized below in claim 20.

Claim 20, as amended, recites (emphasis added):

> 20. A processor for determining a maximum value of a plurality of values stored in source registers and determining an index value of a source register having the maximum value, the processor comprising:
> a destination register;
> a first source register storing a first value;
> a second source register storing a second value;
> means for comparing the first value stored in the first source register with the second value stored in the second source register, ***wherein the first source register and the second source register each include an active status bit to indicate a status of the respective register, and wherein a value of a register having an active status is greater than a value of a register having an inactive status;***
> means for storing the first value in the destination register when the first value is greater than or equal to the second value; and
> means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is greater than the first value.

Applicants have amended claim 20 and canceled claim 25. In rejecting claim 25, the Office Action applies the same rationale used to reject claim 6 and asserts the following: "*Figure 1 with the index field wherein the index field is either exist or non-exist [sic] with the data value to indicate the minimum value within values.*" (Office Action, page 5). Applicants submit that the index field (11b) shown in FIG. 1 of *Okumura* is not equivalent to the recited feature above. In fact, the index field (11b) doesn't appear to

even serve the same function as the active status bit. Applicants refer to the following text passage:

> Accordingly, the numeric data field 11a of the specific register 11 stores the minimum data from among the numeric data previously stored in the registers 5 and 6. Furthermore, the index field 11b of the specific register 11 stores counted results of the counter 9 (i.e., index) corresponding to the minimum data.

(Col. 5, lines 19-24). Rather than indicating whether the value within a given register is greater than the value of another register, the index field (11b) stores counted results of the counter (*i.e.*, index). As such, *Okumura* fails to disclose the features emphasized above in claim 20.

Accordingly, Applicants respectfully submit that independent claim 20 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the highlighted features in claim 20 above.

Dependent Claims 21-24

Applicants submit that dependent claims 21-24 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 32

Applicants respectfully submit that independent claim 32 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the features emphasized below in claim 32.

Claim 32 recites (emphasis added):

32. A method for determining a maximum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:

for each of the plurality of source registers,

comparing a value stored in the source register with a value stored in a destination register;

concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is greater than the value stored in the destination register; and

wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers.

On page 7, the Office Action applies the same rationale used to reject claim 13 to reject claim 32. Applicants respectfully submit that *Okumura* fails to teach the element, "wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers."

As discussed above, *Okumura* specifically teaches that "In FIG. 3, when the operation is started, an initial value is stored in the specific register 11 in step S1. The initial value is the maximum value (0x7FFF) is identical to step S31 described in the background art (FIG. 6)." (Col. 4, lines 53-56). In the background section, *Okumura* teaches that "the initial value is preferably the maximum value within the expressible scope of the numeric data." Applicants submit that this is not equivalent to the element, "wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers," as recited in claim 32 above.

Accordingly, Applicants respectfully submit that independent claim 32 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the highlighted features in claim 32 above.

Dependent Claims 33-35

Applicants submit that dependent claims 33-35 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

III. Response to Claim Rejections Under 35 U.S.C. § 103

Claims 16-19 and 35-38 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Okumura* in view of Applicants' admitted prior art. For at least the reasons set forth below, Applicants traverse these rejections.

Independent Claim 17

Applicants respectfully submit that independent claim 17 patently defines over *Okumura* in view of Applicants' admitted prior art for at least the reason that the combination fails to disclose, teach or suggest certain features in claim 17.

Claim 17 recites (emphasis added):

> 17. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to: compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;
> store the first value in a first destination register of the processor when the first value is less than or equal to the second value; and
> ***store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value, the index value representing the second source register***.

Applicants respectfully submit that the combination of *Okumura* and Applicants' admitted prior art fails to teach the following feature: "store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value, the index value representing the second source register." Specifically, the combination fails to teach of storing an index value in a second destination register. The Office Action relies on the *Okumura* reference to teach this feature and asserts the following: "*corresponding index value of register 6 in Figure 1*." However, this is not equivalent to storing an index value in a second destination register (while the second value is stored in a first destination register). At most, *Okumura* discloses a specific register 11 as shown in FIG. 1. The specific register 11 comprises: a numeric data field 11a and an index field 11b. The minimum data from among all the numeric data is stored in the numeric data field 11a, and the index corresponding to the minimum data is stored in the index field 11b. However, this is not equivalent to storing the second value in the first destination register and an index value in a second destination register of the processor.

Accordingly, Applicants respectfully submit that independent claim 17 patently defines over *Okumura* in view of Applicants' admitted prior art for at least the reason that combination fails to disclose, teach or suggest the highlighted features in claim 17 above.

Dependent Claims 18-19

Applicants submit that dependent claims 18-19 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 36

Applicants respectfully submit that independent claim 36 patently defines over *Okumura* in view of Applicants' admitted prior art for at least the reason that the combination fails to disclose, teach or suggest certain features in claim 36.

Claim 36 recites (emphasis added):

> 36. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and a processor operably connected to the network interfaces and being adapted to:
> compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;
> store the first value in a first destination register of the processor when the first value is greater than or equal to the second value; and
> ***store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the first value, the index value representing the second source register***.

On pages 9-10, the Office Action applies the same rationale used to reject claim 17 to reject claim 36. Applicants submit that the combination of *Okumura* and Applicants' admitted prior art fails to teach the feature emphasized above: "store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the

first value, the index value representing the second source register." Specifically, the combination fails to teach of storing an index value in a second destination register.

The Office Action relies on the *Okumura* reference to teach this feature and asserts the following: "*corresponding index value of register 6 in Figure 1.*" However, as discussed above, this is not equivalent to storing an index value in a second destination register (while the second value is stored in a first destination register). At most, *Okumura* discloses a specific register 11 as shown in FIG. 1. The specific register 11 comprises a numeric data field 11a and an index field 11b. The minimum data from among all the numeric data is stored in the numeric data field 11a, and the index corresponding to the minimum data is stored in the index field 11b. However, this is not equivalent to storing the second value in the first destination register and an index value in a second destination register of the processor.

Accordingly, Applicants respectfully submit that independent claim 36 patently defines over *Okumura* in view of Applicants' admitted prior art for at least the reason that combination fails to disclose, teach or suggest the highlighted features in claim 36 above.

Dependent Claims 37-38

Applicants submit that dependent claims 37-38 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

IV. Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 50-0835.

Respectfully submitted,

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